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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/782,035	02/14/2001	Nixon O	5727	9895

7590 06/18/2003

DORSEY & WHITNEY LLP
1001 PENNSYLVANIA AVENUE
STE. 400
WASHINGTON, DC 20004-2533

EXAMINER
SONG, HOON K

ART UNIT	PAPER NUMBER
2882	

DATE MAILED: 06/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/782,035	O, NIXON	
	Examiner	Art Unit	
	Hoon K Song	2882	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-17 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-17 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 February 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yasuda et al. (US 5949099).

Regarding claim 1, Yasuda teaches a line scan sensor comprising (figure 9):

first and second rows of pixels (figure 9);

corresponding first and second readout registers (figure 9);

a plurality of first channel structures (15a), each channel structure of the first channel structures being disposed between a corresponding pixel of the first row of pixels and a corresponding register element of the first readout register; and

a plurality of second channel structures (15b), each channel structure of the second channel structures being disposed between a corresponding pixel of the second row of pixels and a corresponding register element of the second readout register (column 4 line 28+, figure 9).

Regarding claim 2, Yasuda teaches that a first clocking structure disposed over and transverse to the plurality of first channel structures, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode; and a second clocking structure disposed over and transverse to the plurality of second channel

structures, wherein the second clocking structure includes a transfer gate electrode and a delay well electrode (figure 1 and 2, column 4 line 46+).

Regarding claim 3, Yasuda teaches that the first clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the first clocking structure; and the second clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the second clocking structure (figure 1 and 2, column 5 line 53+).

Regarding claim 4, Yasuda teaches that each pixel of each row of pixels includes one of a photo diode and a pinned photo diode (abstract).

Regarding claim 5, Yasuda teaches that a method of using the sensor comprising steps of

applying a transfer clock pulse to the transfer gate electrode of the first clocking structure and the transfer gate electrode of the second clocking structure;

applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied; and

applying a second delay clock pulse to the delay well electrode of the second clocking structure before the transfer clock pulse is applied (column 5 line 53+).

Regarding claim 6, Yasuda teaches a line scan sensor comprising:

first and second rows of pixels (figure 8);

corresponding first and second readout registers (figure 9);

a first clocking structure disposed between the first row of pixels and the first readout register, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode (figure 1 and 2, column 4 line 46+).

Regarding claim 7, Yasuda teaches that the first clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the first clocking structure (figure 1 and 2, column 5 line 53+).

Regarding claim 8, Yasuda teaches that a second clocking structure disposed between the second row of pixels and the second readout register wherein the second clocking structure includes a transfer gate electrode and a delay well electrode (figure 1 and 2, column 4 line 46+).

Regarding claim 9, Yasuda teaches that the second clocking structure further includes a storage well electrode disposed so that the delay well electrode is located between the storage well electrode and the transfer gate electrode of the second clocking structure (figure 1 and 2, column 5 line 53+).

Regarding claim 10, Yasuda teaches that a plurality of first channel structures coupled between the first row of pixels and the first readout register, each channel structure of the first channel structures being disposed under and transverse to the first clocking structure and between a corresponding pixel of the first row of pixels and a corresponding register element of the first readout register; and a plurality of second channel structures coupled between the second row of pixels and the second readout register, each channel structure of the second channel structures being disposed under

and transverse to the second clocking structure and between a corresponding pixel of the second row of pixels and a corresponding register element of the second readout register (figure 1 and 9).

Regarding claim 11, Yasuda teaches that of applying a transfer clock pulse to the transfer gate electrode of the first clocking structure and the transfer gate electrode of the second clocking structure; applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied; and applying a second delay clock pulse to the delay well electrode of the second clocking structure before the transfer clock pulse is applied (column 5 line 53+).

Regarding claim 12, Yasuda teaches that applying a transfer clock pulse to the transfer gate electrode of the first clocking structure; and applying a first delay clock pulse to the delay well electrode of the first clocking structure after the transfer clock pulse is applied (column 5 line 53+).

Regarding claim 13, Yasuda teaches that each pixel of each row of pixels includes one of a photo diode and a pinned photo diode (abstract).

Regarding claim 14, Yasuda teaches a line scan sensor comprising: first and second rows of pixels (figure 9); a delay register coupled to the first row of pixels; a first readout register coupled to the delay register; and a second readout register coupled to the second row of pixels (figure 1 and 2, column 4 line 46+).

Regarding claim 15, Yasuda teaches a summation circuit to combine serial outputs from the first and second readout registers (figure 9).

Regarding claim 15, Yasuda teaches that each pixel of the first and second row of pixels includes one of a photo diode and a pinned photo diode (abstract).

Regarding claim 17, Yasuda teaches 17. The sensor of claim 14, wherein each pixel of the first and second row of pixels includes a storage well and one of a photo diode and a pinned photo diode (figure 1 and 2).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 6 and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirama et al (US 6028299).

Regarding claims 1, 6 and 14, Hirama teaches a line scan sensor comprising:

first and second rows of pixels (figure 1);

corresponding first and second readout registers (figure 1);

a first clocking structure disposed between the first row of pixels and the first readout register, wherein the first clocking structure includes a transfer gate electrode and a delay well electrode (figure 1, column 3 line 32+).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hoon Song whose telephone number is 703-308-2736. The examiner can normally be reached on 8:30 AM - 5 PM, Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on 703-305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4858 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

DAVID V. BRUCE
PRIMARY EXAMINER

Hoon Song
June 5, 2003